Electronic Version
Stylesheet Version v1.1.1

[DYNAMIC SEMICONDUCTOR MEMORY DEVICE AND BIT LINE PRECHARGE METHOD THEREFOR]

Abstract

A dynamic semiconductor memory device capable of reducing standby current is disclosed. In a standby mode wherein only a refresh operation is performed, a precharge/equalize signal is activated only during a predetermined period before a word line is activated so as to precharge a bit line pair to a voltage that is half a line voltage immediately before the word line is activated. In the standby mode, the bit line pair is electrically isolated from a regulator that generates a voltage that is half the line voltage except for the above predetermined period, thus preventing leakage current from flowing therebetween even if a defect in which the word line is shorted with the bit lines occurs.